

Ultra-low power 32-bit Arm® Cortex®-M3, 16-bit NXP CoolFlux DSP, 512 kB Flash, 128 kB SRAM, on-chip DC-DC converters and 4 channel ADC

Features

- **Arm Cortex-M3 32-bit CPU**
 - Operating frequency up to 100 MHz
 - 1.8 V to 3.6 V power supply
 - 1.24 DMIPS/MHz
 - 800nA sleep mode + RTC on
 - ~13 uA/MHz run mode
 - NVIC with 24 interrupts
 - Serial Wire Debug support
- **Memory**
 - 512 kB embedded nonvolatile FLASH
 - 128 kB SRAM
 - 8 kB BootROM
- **NXP CoolFlux DSP16**
 - Ultra-low power 16-bit DSP
 - Operating frequency up to 60 MHz
 - Dual 16x16 MAC
 - 3 pipeline stages
 - 32 kB program memory and 32 kB data memory
 - 4 channel DMA
- **Clocks**
 - Integrated 32 kHz oscillator
 - Integrated 8 MHz high frequency oscillator
- **OS timer**
 - 64-bit counter
 - 4 comparators + overflow with interrupts
- **Real time clock**
 - Watchdog timer interrupt or reset
- **Power management control unit**
- **8 channel PWM**
 - Supports frequencies up to 4 MHz
- **32 GPIOs**
- **UART (2X)**
 - Supports baud rate up to 460,800
 - Optional Hardware flow control (RTS/CTS)
- **SPI master (2X)**
 - Supports frequencies up to 4 MHz
 - SPI modes: 0,1,2,3 (LSB or MSB)
- **I2C master (2X)**
 - Supports standard (100 kb/s) and full (400 kb/s) transfer rates
- **I2S**
 - Supports mono or stereo input and output at 8, 16 or 32 kSPS
- **2 channel 12-bit 200 kSPS ADC**
 - 1 uW typical power consumption for 200 kSPS continuous conversion
- **On-chip analog blocks**
 - Ultra-high efficiency buck converters
 - Power on reset
 - Temperature Sensor
- **QFN-88 (10x10) package**
 - Smaller QFN and CSP in development

ECM3531 Block Diagram

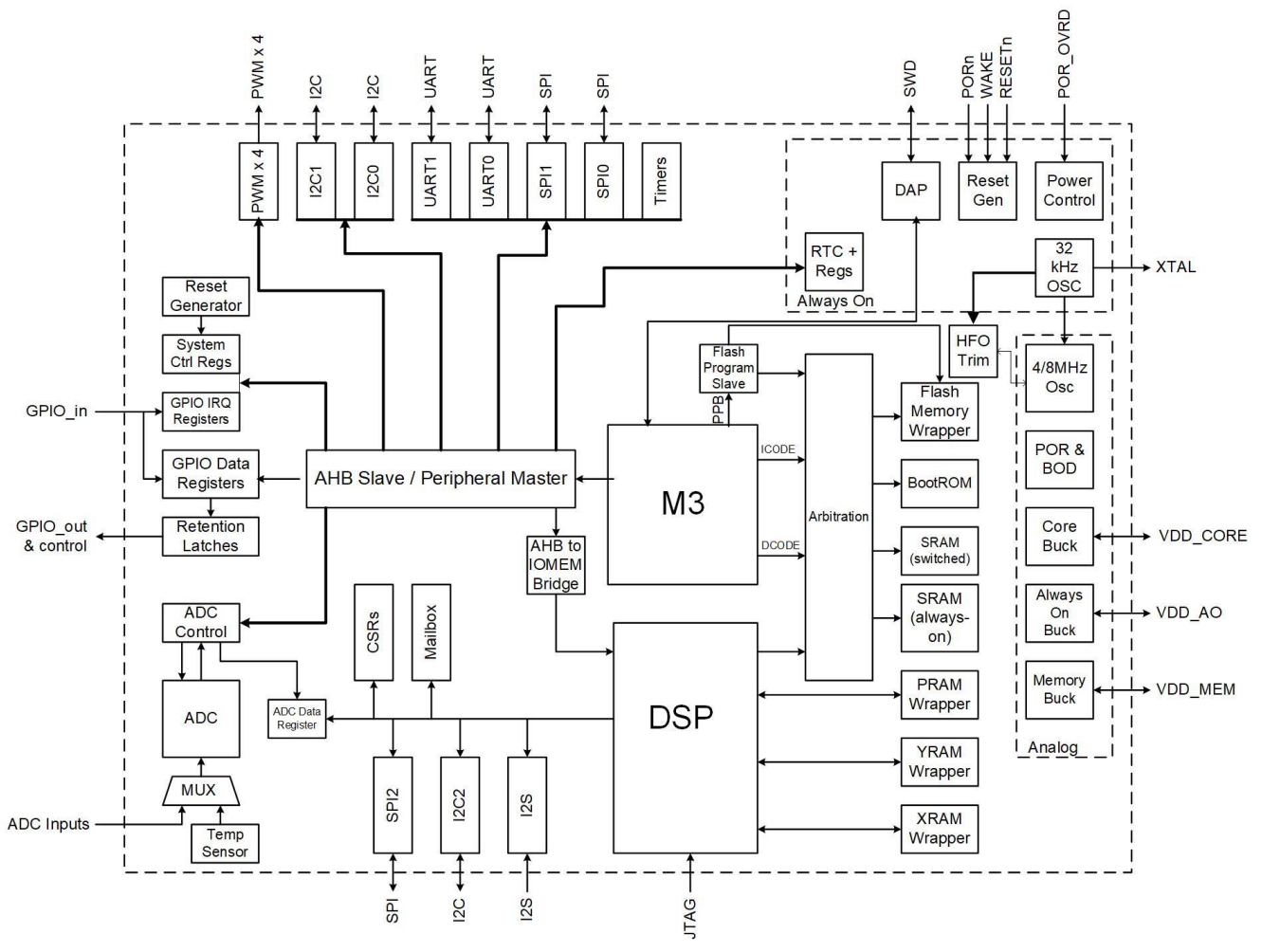


Figure 1 ECM3531 Chip Block Diagram

ECM3531 Chip Pinout

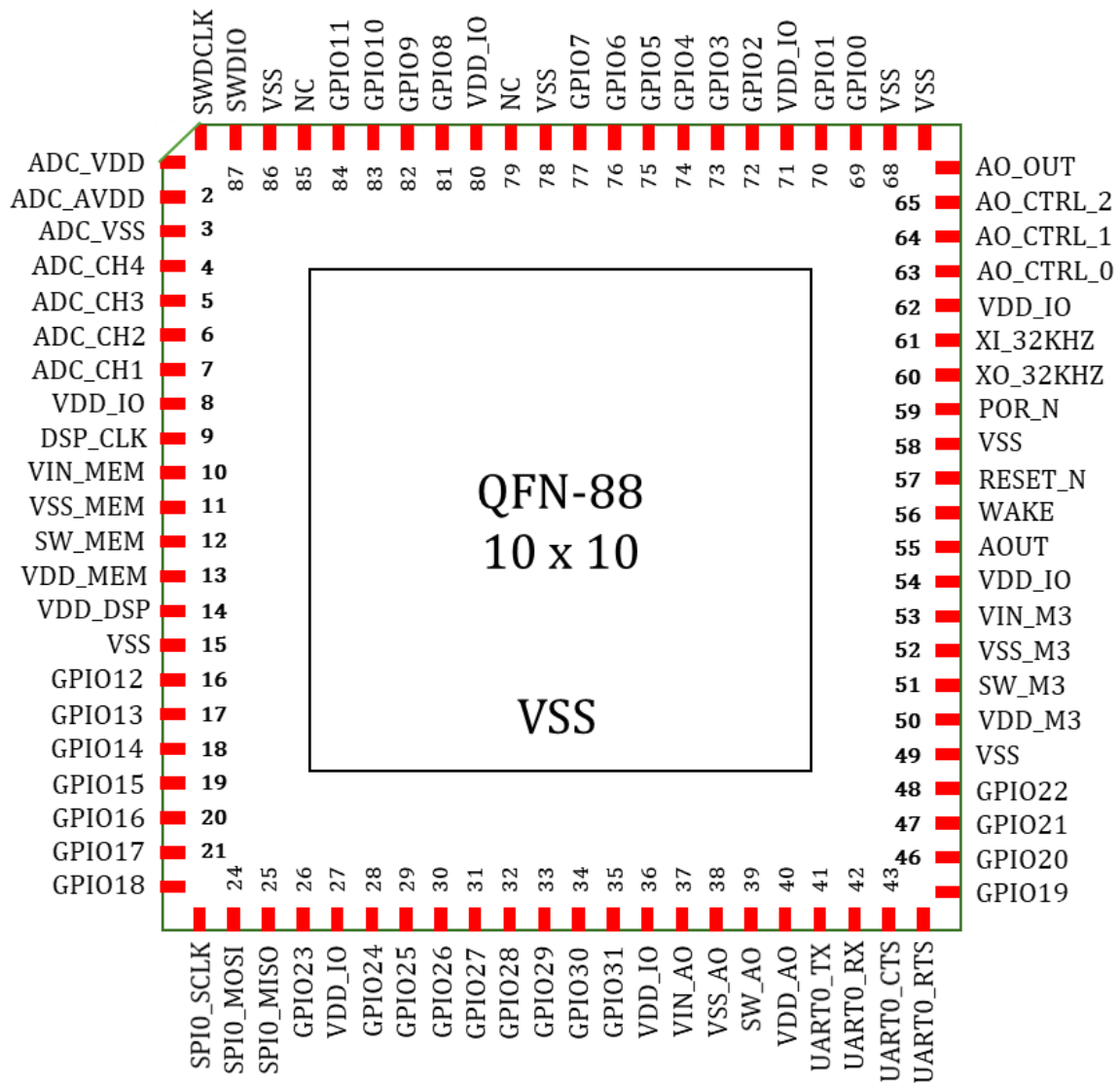


Figure 2 ECM3531 Pinout

Revision History

Date	Version	Changes
July 20, 2018	0.1	Created
July 25 th , 2018	0.2	Diagram
Aug 14 th , 2018	0.3	Updated Spec
Aug 20 th , 2018	0.4	Updated Diagram
Sept 6 th , 2018	0.5	Updated Features
Oct 16 th , 2018	0.7	Updated Features